REMARKS

Claims 1-22 are pending in the application. Claims 1, 2, 4, 6, 8, 9, 11, 12, 14, 16, 17, 20 and 22 are rejected. Claim 8 is herein amended.

Drawings

The Examiner asserts the Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Applicants include a replacement sheet for Figure 8.

Specification

The Examiner asserts that the recitation of the circles in Figs. 5 and 6 (page 13) is not illustrated. Applicants assume that the Examiner simply does not see the small black circles in the drawings figures. Applicants herein clarify the circles in Figure 6 by submitting replacement sheet for Fig. 6.

The Examiner asserts that the disclosure should describe the steps of forming a compound semiconductor film that contains Si and another semiconductor element, and has a composition with a high content of silicon in an upper layer region and a lower layer region, and a high content of the other semiconductor element in an intermediate layer region, as recited in claims 1 and 8.

Applicants respectfully disagree with the objection, because one skilled in the art would have immediately recognized how to perform the steps of forming a compound semiconductor film (SiGe/SiGeC film 9). Applicants submit herewith the attached document, which shows that as of 1994, the detailed manufacturing steps and the basic structure of the compound semiconductor film (SiGe/SiGeC film 9) in the specification, because they had been already

known to the public before August 30, 2002 (the priority date of the present application). In the attached document, Fig. 2 shows a device structure, and its manufacturing method is explained in paragraphs 2 and 3.

Correction to Claim 8

Applicants note that the previous amendment appears to have introduced a typographical error in claim 8. That is, Applicants apparently deleted the word "opening" in the third line. Applicants reinsert this term herein.

Claim Rejections - 35 U.S.C. §103

Claims 1-2, 4, 6, 8-9, 11-12, 14, 16-17, 19-20 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Asai et al. (U.S. Patent No. 6,713,790) in view of Applicant's admitted prior art (AAPA).

The Examiner notes that Asai et al. does not teach a compound semiconductor film having upper layer region, a lower layer region, and an intermediate region having the relative contents of the semiconductor elements. The Examiner notes that the present specification teaches in pages 2-3 that it is conventional to obtain a compound semiconductor film which contains silicon and another semiconductor element, and has a composition with a high content of silicon in an upper layer region and a lower layer region, and a high content of the other semiconductor element in an intermediate layer region. The Examiner concludes that it would have been obvious to use a compound semiconductor film having a composition with a high content of silicon in an upper layer region and a lower layer region, and a high content of the

other semiconductor element in an intermediate layer region in the device of Asai et al. in order to simplify the processing steps of making the device by using a conventional processing method.

Applicants respectfully disagree with this rejection, because even if the references were combined, not all of the claimed limitations are taught or suggested by cited combination.

By way of explaining the present invention, after a multilayer film having an opening is formed a compound semiconductor film is formed on the entire surface of the multilayer film. As a result, as shown Fig. 2A, the compound semiconductor film is formed on the bottom surface part of the opening, on the side wall part of the opening, and on the upper surface part of the multilayer film. Then, anisotropic dry etching is performed for the formed compound semiconductor film so as to reach a certain height of the opening. As a result, as shown in Fig. 3B, the compound semiconductor film remains up to the certain height of the side wall part of the opening and on the bottom surface of the opening.

By this method, a compound semiconductor film in the present invention has a composition with a high content of Si in its upper layer region and lower layer region and a high content of the other semiconductor element in an intermediate layer region. For example, in Fig. 2A, a compound semiconductor film is formed horizontally to a semiconductor substrate 1 on the bottom surface of an opening and on the upper surface of a multilayer film. The compound semiconductor film that is formed horizontally to a semiconductor substrate 1 has a composition with a high content of Si at the part close to the contact surface with the bottom surface of the opening and at the part close to the exposed surface that is horizontal to the semiconductor substrate 1, and a high content of the other semiconductor element, such as Ge, in an intermediate layer region, which corresponds to the intermediate part of the contact and exposed surfaces. Meanwhile, on the side wall part of the opening, a compound semiconductor film is

formed vertically to a semiconductor substrate 1. The compound semiconductor film that is formed vertically to the semiconductor substrate 1 has a composition with a high content of Si at the part close to the contact surface with the side wall of the opening, and at the part close to the exposed surface that is vertical to semiconductor substrate 1, and a high content of the other semiconductor element such as Ge, in an intermediate layer region that corresponds to the intermediate part of the contact and exposed surfaces.

With the compound semiconductor film formed as explained above, when anisotropic dry etching is performed for the compound semiconductor film so as to reach a certain height of the opening, as shown in Fig. 3B, a compound semiconductor film remains only up to a certain height of the side wall of the opening and on the bottom surface part of the opening.

As described above, a compound semiconductor film that is in contact with a side wall of an opening has a composition with a high content of Si at the part close to the contact surface with the side wall of the opening, and at the part close to the exposed surface which is vertical to a semiconductor substrate 1, and a high content of the other semiconductor element, such as Ge, in an intermediate layer region which corresponds to the intermediate part of the contact and exposed surfaces. Under the condition that the content rate of the each semiconductor element (Si, Ge and the like) is different in the horizontal direction to a semiconductor substrate 1, when isotropic etching is performed for a compound semiconductor film so as to reach a certain height of the opening, as shown in the circle in Fig. 5 for example, clearances occur in the intermediate layer region of the compound semiconductor film which is in contact with the side wall of the opening, because of the difference in the etching rate of Si and the other semiconductor element such as Ge. Due to the clearances, electrical connection of the bass electrode, the P diffusion

region and the base electrode is hindered, making it impossible to meet the transistor property which is initially expected.

Applicants note that in contrast, Asai et al. disclose completely different steps of manufacturing a semiconductor. A compound semiconductor film 111 of Asai et al. is formed prior to a multilayer film 115, 117, and 120 and located at a lower side of the multilayer film 115, 117, and 120 (Fig. 10a for example).

On the other hand, a compound semiconductor film of the present invention is formed after a multilayer film is formed. Thus, it is formed at the upper side of the multilayer film. After that, anisotropic dry etching is performed for the compound semiconductor film. As a result, the compound semiconductor film is formed at the position of the fourth oxide film 120 of Asai et al. if the compound semiconductor film of the present invention corresponds to the composition shown in Fig. 10a of Asai et al. In this way, the present invention is based on the premise that etching is performed for a compound semiconductor film which is in contact with the opening so as to reach a certain height of the opening.

The Examiner asserts that Asai et al. disclose that anisotropic dry etching is performed for a compound semiconductor film 111 so as to reach a certain height of the opening. However, as described in the column 20, line 19-27, and column 20, line 29-36, anisotropic dry etching is performed not for the compound semiconductor film 111, but for polycrystalline silicon film, the second oxide film 112 and the fourth oxide film 120. Accordingly, the composition of the Asai et al. is completely different from that of the present invention.

Further in the present invention, the compound semiconductor film, which is formed up to a certain height of the opening after manufacturing steps that are the premise of the present invention as described above, changes in the content rate of the each semiconductor element in

the horizontal direction to a semiconductor substrate 1, at the part that is in contact with the opening. When the content rate of each semiconductor element is different in the horizontal direction, likewise, the etching rate also changes in the horizontal direction. Accordingly, when isotropic dry etching is used, clearances occur in the intermediate layer region of the compound semiconductor film that is in contact with the side wall of the opening. The present invention provides a solution to this problem by using anisotropic dry etching.

In contrast, as described earlier, anisotropic dry etching of Asai et al. is not for a compound semiconductor film. Thus, the etching rates of the each semiconductor element in a compound semiconductor film cannot be made substantially uniform, differing from the present invention.

Moreover, in the AAPA, anisotropic dry etching is not performed for a compound semiconductor film. In this way, there is a clear difference between the present invention, and Asai et al. and AAPA. Therefore, one skilled in the art at the time of filing of the application would not have conceived of the composition of the present invention by referring to Asai et al. and AAPA.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

Kenneth H. Salen
Attorney for Applicants
Registration No. 43,077
Tel: 202-822-1100
Fax: 202-822-1111

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Enclosures: Replacement drawing sheets for Figs. 6 and 8

Si/$Si_{1-x-y}Ge_xC_y$/Si Heterojunction Bipolar Transistors, L.D. Lanzerotti, A. St. Amour, C.W. Liu, and J.C. Sturm, pp. 930-932, 1994 International Electron Devices Meeting, San Francisco, CA, USA, December 11-14, 1994. Solid State Devices-SiGe and Novel Devices Chair(s): Steve Mittleman, USAF Rome Laboratory; K.L. Wang, UCLA

Si/$Si_{1-x-y}Ge_xC_y$/Si Heterojunction Bipolar Transistors

D. Lanzerotti, A. St.Amour, C.W. Liu*, and J.C. Sturm
:pt. of Electrical Engineering, Princeton University, Princeton, NJ 08544
urrent address: Dept. of Electrical Engineering, National Chunghsing University, Taichung, Taiwan 40227

Recently, great interest in silicon-based heterojunction devices has been caused by high-speed $Si_{1-x}Ge_x$ se HBTs with f_t exceeding 100 GHz. [1, 2] To extend silicon heterojunction technology beyond strained $_{1-x}Ge_x$, several groups have pursued $Si_{1-x-y}Ge_xC_y$ alloys, which are of interest because carbon is expected to ow the possibility of strain-free silicon heterostructures which will eliminate a major constraint on device design. veral groups [3,4] have succeeded in growing strain compensated $Si_{1-x-y}Ge_xC_y$ layers on silicon, but to date re have been no $Si_{1-x-y}Ge_xC_y$ electrical devices of any kind or experimental bandgap studies reported. In this per we present the first electrical devices of any kind containing $Si_{1-x-y}Ge_xC_y$ alloys and present preliminary asurements of $Si_{1-x-y}Ge_xC_y$ bandgaps. Temperature studies of these devices indicate that the partially strain mpensated $Si_{1-x-y}Ge_xC_y$ bandgap remains comparable to the bandgap of strained $Si_{1-x}Ge_x$, a most surprising d formitous result.

The epitaxial layers were grown by rapid thermal chemical vapor deposition (RTCVD). The base layers re grown at 550°C using a mixture of DCS, germane, diborane, and methylsilane (the carbon precursor). The itter was then grown at 700°C using silane and phosphine. Four device structures were fabricated with different els of C in the base while holding the Ge content fixed. Figure 1 shows x-ray diffraction (XRD) spectra from : four HBT structures. The base of the control device (1665) contained 25% Ge and no C. As C was added, note it the peak of the strained $Si_{1-x-y}Ge_xC_y$ layers moved towards the Si substrate peak, indicating a reduction of ain. From Fig. 1, C fractions of 0.001, 0.007, and 0.011 were estimated for samples 1673, 1675, and 1676, pectively.

Double-mesa transistors (Fig. 2) were fabricated by a very simple three mask process using a combination selective wet and dry etching designed to examine the transport of electrons in the base and to determine the idgap of the base, not for high performance. Figure 3 shows the I-V characteristics of the BE and BC diodes m the device with 0.7% C. Figure 4 shows the HBT characteristic from the same sample (0.7% C), showing ll behaved transistor characteristics with $V_A > 100V$ and a $V_{B,CEO} = 5V$. The low gain (~2.5) was limited by assive base current, presumably due to recombination at the unpassivated mesa edges. Note that the collector rent, which depends on transport across the $Si_{1-x-y}Ge_xC_y$ base, was ideal (see Gummel plot, Fig. 5).

Figure 6 shows the ratio of the collector currents in devices with 0.7% and 1.1% C in the base to that of control device as a function of inverse temperature. Using this standard technique for narrow base HBTs [5], slope can be used to give the difference in bandgap of the base regions. The curves are nearly flat, indicating t the bandgap of the $Si_{1-x-y}Ge_xC_y$ alloys did not increase as C was added. This indicates that it should be sible to grow completely strain-free $Si_{1-x-y}Ge_xC_y$ structures which still have a substantial bandgap reduction mpared to Si. The HBT results are consistent with photoluminescence of similar $Si_{1-x-y}Ge_xC_y$ layers grown in : lab (Fig. 7), which also show that the bandgap of strained $Si_{1-x-y}Ge_xC_y$ on Si does not increase as C is added. ese results appear to be consistent with the theoretical calculations of Ref. 6 which predict a surprisingly low idgap for dilute C alloys due to strong atomic relaxation around certain substitutional C sites.

In summary, we have demonstrated the first electrical devices of any kind in the $Si_{1-x-y}Ge_xC_y$/Si erojunction system. The HBTs demonstrated the potential promise of this new material system and also show t it may be possible to achieve a significant bandgap offset relative to silicon with a strain-free material.

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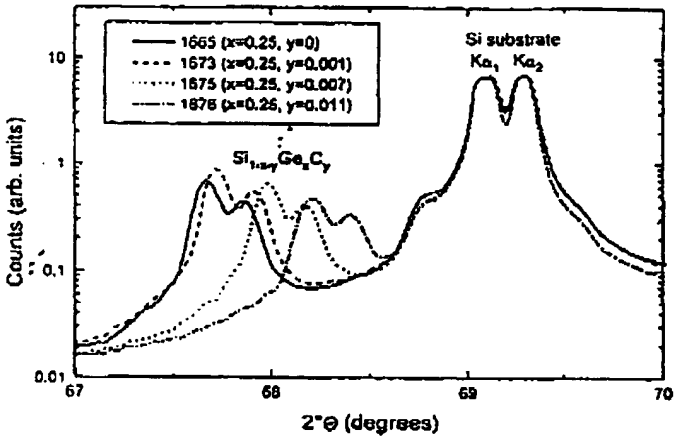

Fig. 1. X-ray diffraction spectra from four SiGeC HBT structures.

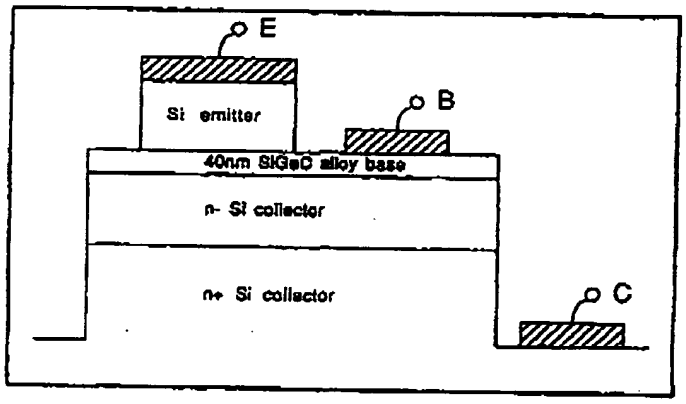

Fig. 2 Cross section of the SiGeC HBT structure.

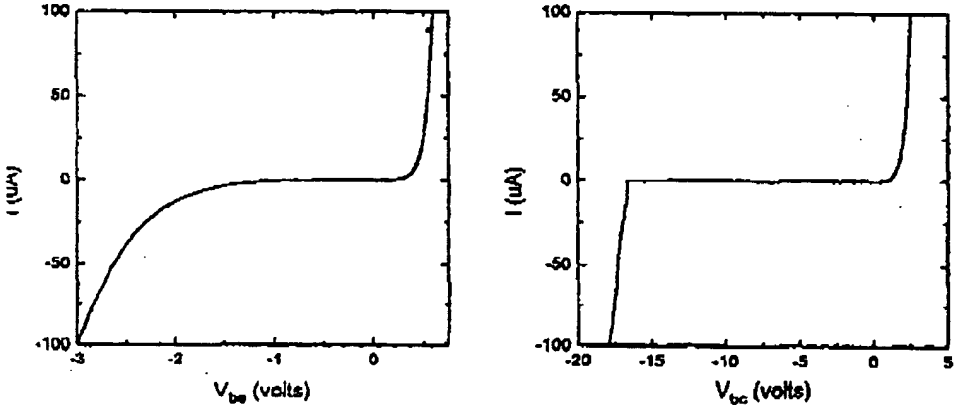

Fig. 3. Emitter-base and collector-base diodes of SiGeC HBT with 0.7% C in the base.

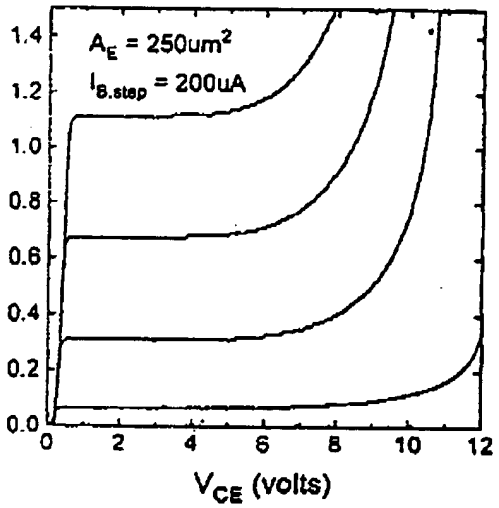

Fig. 4. Common-emitter characteristics of SiGeC HBT with 0.7% C in the base.

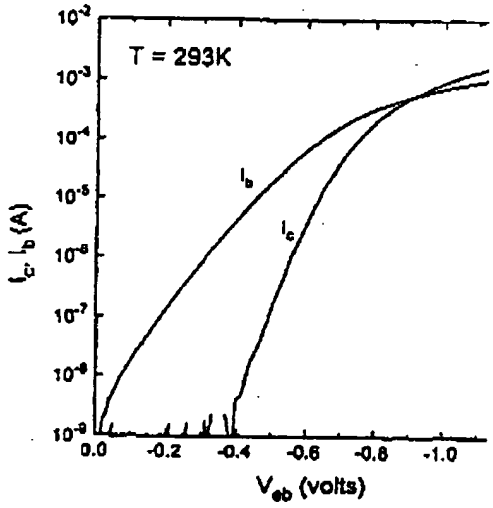

Fig. 5. Gummel plot of SiGeC HBT
0.7% C in the base.

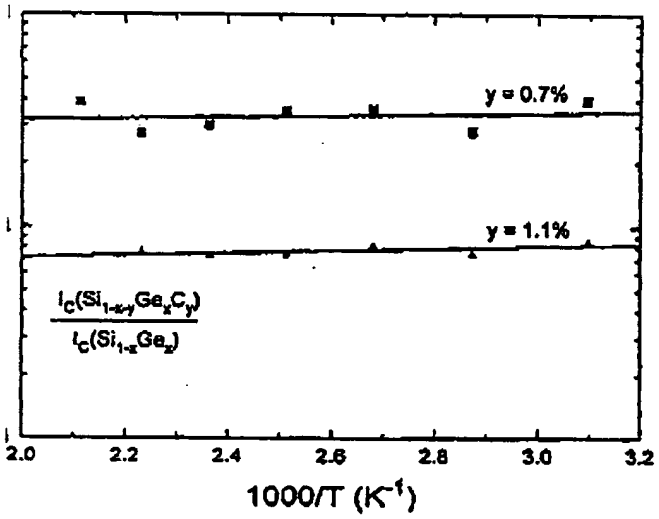

Fig. 6. Normalized collector current vs. inverse temperature from two SiGeC HBTs.

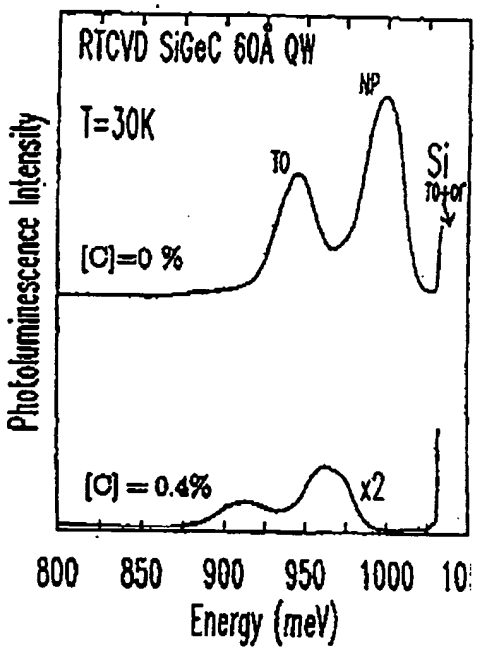

Fig. 7. Photoluminescence spectra from two quantu